

Design Methodology

(System and Logic Design with VHDL)

The main goal of this short course is to present a new methodology for system and logic design of very complicated digital systems. This methodology is based on Algorithmic State machine (ASM) transformations (composition, minimization, extraction, etc.), special algorithms for Data Path and Control Unit design and a very fast optimizing synthesis of FSMs and combinational circuits with hardly any constraints on the number of inputs, outputs and states. Such high level synthesis allows very fast to implement, check and estimate many possible design versions, to find an optimized decision of the design problem and to simplify the verification problem for digital systems.

Each step of system design in this short 16-hour course will be supported by new EDA tool "Abelite", designed by author.

Algorithmic State Machines (ASM) and Finite State Machines (FSMs). Flowcharts and Algorithmic state machines. Synthesis of FSM Mealy, Moore and their combined model. Synthesis of logic circuits for control FSM. Transformation of ASM: minimization, composition, decomposition etc.

Multilevel and Multioutput Synthesis. Factoring. Multilevel minimization of logic circuits with a large number of inputs and outputs. Factoring and term decomposition in multilevel and multioutput logic circuits.

Functional design of digital system. Functional ASMs for constituent subbehaviors. Combined functional ASM. Functional simulation of a digital system.

Data path synthesis. Design process. Process table, connection graph and list of parallel microoperations. Graph of incompatibility. Bus optimization. Formal synthesis of data path. VHDL code for data path. Formal methods for design of test benches for data paths.

Control Unit synthesis. Transformation of functional ASM into structural ASM. Output signal optimization. Synthesis of Finite State Machine (control unit). Top level design. VHDL code for the top level.

Samary Baranov, Logic and System Design of Digital System. The book will be published in 2007.

Prof. Samary Baranov